A Highly Integrated UHF Data Receiver for Vehicle Applications

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Abstract **This paper describes a UHF data receiver designed for short range data transfer for automotive applications: keyless entry and tyre pressure monitoring systems in the 315, 434 and 868MHz bands. Received signals may be OOK or FSK modulated and may come from transmitters which are PLL-tuned (i.e. precise) or SAW-tuned (less precise, requiring a wide bandwidth receiver). The design target may be summarised as: a very high level of integration and autonomy combined with best possible performance (for example, -107dBm sensitivity), consuming from 5mA at 434MHz to 7mA at 868MHz. This has been achieved by a superheterodyne architecture which has an image cancelling mixer, a fully integrated IF filter and a fully integrated local oscillator and PLL. A digital control block permits configuration of the circuit and some signal processing. The wake-up time is short so the average current consumption may be user-defined by an awake/sleep cycle.**

I. INTRODUCTION: TECHNOLOGY and ARCHITECTURE

The choice of the circuit architecture was driven by the targets of high performance, high-level integration and low power consumption outlined in the abstract. The technology used is a 0.6um BiCMOS process with NPN's having an fT of 20GHz, polysilicon resistors, dense capacitors but no integrated inductors.

The need to receive OOK-modulated data eliminates the possibility of using a 'zero-IF' architecture which would have been attractive for FSK because of the easy integration of low-pass filters for selectivity. Nonetheless, it was decided to integrate the IF filter, primarily for cost reasons: on a dense process the area of the filter does not significantly exceed that of the pads which would be needed to connect to an external passive filter. Additionally, readily available ceramic filters require matching to impedance levels which are inconveniently low for low current IC design. A high-performance integrated filter must however operate at a low centre frequency. The frequency chosen was 660kHz. This choice is linked with that to use an image-cancelling mixer: in this way the use of a front-end SAW filter for channel selectivity becomes optional. Without such a filter image rejection of 25dB may be expected, however if a front-end SAW filter is used there is useful additional attenuation of an image 1.32MHz away from the wanted signal. The bandwidth of the IF filter may be programmed to 300kHz or 500kHz by metal option; it is a 4th order Butterworth implemented as a matched LC ladder in which the inductors are realised by gyrators.

The choices made for the IF filter define the requirements on other circuit blocks. The dynamic range of the filter, 66dB, is less than the linear operating range required of the receiver. Therefore an AGC is used on the LNA preceding the mixer which gives a total signal handling range of 100dB.

In the post-filter blocks further AGC controlled amplification is provided, followed by demodulators for both OOK and FSK modulated data and a comparator which interfaces between the analogue radio and the digital backend.

The absolute frequency of all integrated filter blocks is tuned by controlling the phase of a bandpass filter to be exactly 90 degrees when passing a signal obtained from the crystal oscillator used to tune the local oscillator.

The fully integrated local oscillator has been implemented with a relaxation oscillator. The phase noise near the oscillation frequency may be reduced by the PLL loop, tuned by a crystal oscillator. The I/Q signals required for the image-reject mixer are obtained both at UHF and IF by passive all-pass networks.

At the backend of the receiver a versatile digital block permits soft configuration of the circuit, recognition of valid received data and recovery of a clock from Manchester-coded data.

Figure 1 shows a block diagram of the receiver.

II. MIXER and IF FILTER

The image cancelling mixer comprises 2 mixers driven in quadrature such that after phase shifting one of the IF output signals by 90 degrees and summing, the wanted signal is recovered while the image is rejected [1].

In Figure 2 the principal elements of the image cancelling mixer are shown; for clarity, biasing and buffers between stages are omitted. Up to 20dB of gain are provided by the LNA formed by Q1 and its load R2. The mixer AGC reduces the gain of this stage by diverting current from Q3, which normally acts as a cascode, into Q2. The diverted current is recombined in R3 so that R1 defines the input impedance without adding significant front-end noise. The real part of the input impedance is R1/(1 + G) where G is the gain to the bottom of R3.

Q4-Q7 and M1, M2 form two classic 4-quadrant mixers, although the LNA gain requires that they be linearised by R4-R7. RP1, CP1, RP2, CP2 together with the antiphase signals driving them form all-pass networks. The ratio between their tuning frequencies is about 6, centred on the

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IF frequency of 660kHz. The phase difference between their outputs IF 'I' and 'Q' is a good approximation to 90degrees over a wide frequency range around 660kHz - though in practice it is necessary to use two cascaded networks similar to those shown but with staggered tuning to obtain fabrication process independent IF I/Q signals over a wide enough frequency range.

The loads shown as Z1-Z6 have a low DC impedance and a high AC impedance, and do not otherwise participate in the circuit function. The IF I and Q signals are summed in the amplifier formed by Q8 and Q9 and passed as an output current to the IF filter. The voltage at the IF filter input is sensed and used to control the mixer AGC.

The mixer block provides 50dB of gain between RFIN and the IF filter; the noise figure is 5dB but the system noise figure is improved by 3dB compared with a non- image cancelling mixer since the image noise is rejected. Its current consumption is 1.25mA.

The IF filter is an implementation of a lossless LC ladder filter in which gyrators are used both to realise the inductors and to perform conversion between series and parallel networks. The structure is therefore fully differential, giving good immunity to interfering signals and high signal handling capability - see Figure 3. The filter is a 4th-order Butterworth transformed to give a bandpass characteristic. The input and output matching resistances RIN and ROUT are realised with single transconductance stages identical to those of the gyrators with the output simply connected to the inputs. The filter bandwidth may be adjusted to match different types of transmitter simply by altering (by metal option) the values of the capacitors used directly in the filter and in the gyrators for the inductances.

M1 and M2 are the differential input pair, degenerated by M3 and M4 which are acting as voltage controlled resistors to tune the filter by altering the effective inductance value. Their resistance value is set by an AFC loop in which a second order bandpass filter made with blocks identical to those of the IF filter is tuned using a signal obtained from the PLL crystal oscillator: the reference frequency is forced by local negative feedback to establish a 90 degree phase shift in the AFC filter. Common mode feedback is provided locally via M5 and M6. The overall bias is furnished by Vbias, whose value is established to give the wanted operating point in a dummy gyrator outside the filter itself.

The 4th-order Butterworth IF filter has a signal handling capability of 300mVrms; its input related noise is 170uVrms and it consumes 700uA including the tuning loop.

III. IF AMPLIFIER and DEMODULATION

The IF amplifier provides about 55dB of gain; sufficient to permit detection of amplitude modulated data in the data slicer at the expected limit of sensitivity. Although AM data is in principal OOK modulated, the modulation depth will be less than 100%, either due to imperfect modulation in the transmitter or due to interfering in-band signals. Therefore an AGC system which can reduce the gain to maintain linearity is required.

For FSK demodulation the IF AGC is disabled and an amplitude limited signal is connected to a bandpass filter tuned to about 850kHz, just above the IF pass-band, made with the same elements as the IF filter. This performs FM to AM conversion, after which the signal is fed back into the normal AM channel for detection by a classical diode detector.

After the AM signal has been detected it is filtered by a fully integrated untuned two-pole filter, then converted to a digital signal in a comparator. When OOK-modulated data is received the control of the amplitude of the AM signal by the AGC system permits a fixed comparison level. With FSK-modulated data, both the mean value and amplitude of the AM signal after FM to AM conversion vary with the frequency deviation and the actual IF frequency. Therefore the comparison level used is the AM signal mean value. Since the IF AGC is disabled when FSK data is received, the AGC pin and external capacitor may conveniently be used to store this comparison level.

IV. VCO and PLL

The local oscillator is tuned to the required frequency by dividing by 32 and 64 in the 300-450MHz and 868MHz bands respectively and comparing the divided frequency with that of a crystal oscillator at 10-13MHz.

The local oscillator used is a relaxation oscillator and is similar to a classical emitter coupled oscillator in which many precautions were taken to reduce phase noise. Although the intrinsic phase noise of a relaxation oscillator is higher than that of an LC oscillator running at a similar current, it does in fact present a number of advantages in the present receiver, in particular that of being easily usable over the entire 300MHz to 900MHz range. The tuning of the oscillator by the PLL is achieved simply by generating a current in response to a control voltage.

The phase noise of the oscillator is -88dBc/Hz at a 500kHz offset from 868MHz. This is satisfactory in some applications, such as 'in-car' applications like tyre pressure monitoring. Where more robust performance is required the phase noise of the oscillator may be improved within a MHz or so of the oscillation frequency by using a wide-band PLL. Theoretically a 2nd order 1.5MHz PLL loop will give a phase noise improvement of 19dB at 500kHz, although the low current levels at which the receiver operates have permitted somewhat less improvement than this due to noise in the reference oscillator and UHF divider chain.

Special simulation techniques were developed to simulate the noise in the PLL loop. For example, the amplitude noise of a highly non-linear phase-frequency detector, which is of classical design [2], is important since this translates into VCO phase noise. It was evaluated by allowing the PLL to stabilise in simulation using a behavioural VCO and evaluating and integrating the noise at the PLL filter at each timestep of the transient analysis. Figure 4 shows an example of such a simulation in which it can be seen that although most of the noise is generated when the PFD switches, there is a non-negligible contribution outside of this time, due mainly to PNP sources which are too slow to switch completely off.

The complete VCO, PLL and I/Q phasing networks to drive the mixers consume about 2mA.

V. Digital Back-End Circuits

The CMOS logic density of 6000 gates/mm^2 enables the integration of a versatile digital block.

The receiver communicates with the microcontroller through a standard serial peripheral interface (SPI). In this way, a high level of software programmable configuration flexibility is reached. The main parameters that can be set are: the modulation type, the data rate, an ID byte and the wake/sleep cycle timing. A power-on-reset sets the circuit in the most commonly used configuration, so programming is optional. The SPI is also used to send out received data.

A state machine combined with a low current strobe oscillator controls the wake/sleep cycling. A data processor performs clock recovery from Manchester-coded data and detection of a programmable ID byte so that only valid data are sent out. This reduces the global current consumption by avoiding waking up the microcontroller for processing irrelevant received data.

Great care was taken to prevent any degradation of the receiver's performance due to switching spikes in the digital part. It has its own supply pins. On chip substrate connections wired to a dedicated pin collect any substrate current injected by the noisy modules.

100% testability of the digital part has been achieved by using scan path methodology.

VI. Conclusion

A highly integrated UHF data receiver has been developed and is now being qualified. The total current consumption for a -107dBm sensitivity is 5mA at 434MHz and 7mA at 868MHz, though this may be reduced to as low as 0.3mA by wake/sleep cycling. Figure 5 shows the receiver sensitivity in an application in which a narrow band PLL is used, and Figure 6 shows an application circuit in which the only mandatory expensive external component is the crystal. The complexity of implementing the radio receiver has been integrated into the IC, leaving a very simple application design for the end user.

Acknowledgements

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References

[1]. For example, Lee, T. H., The Design of CMOS RF Integrated Circuits; Cambridge University Press, UK, 1998. Chapter 18.

[2]. Gardner, F. M., Phaselock Techniques; John Wiley & Sons, New York, 1979. Figure 6.18.

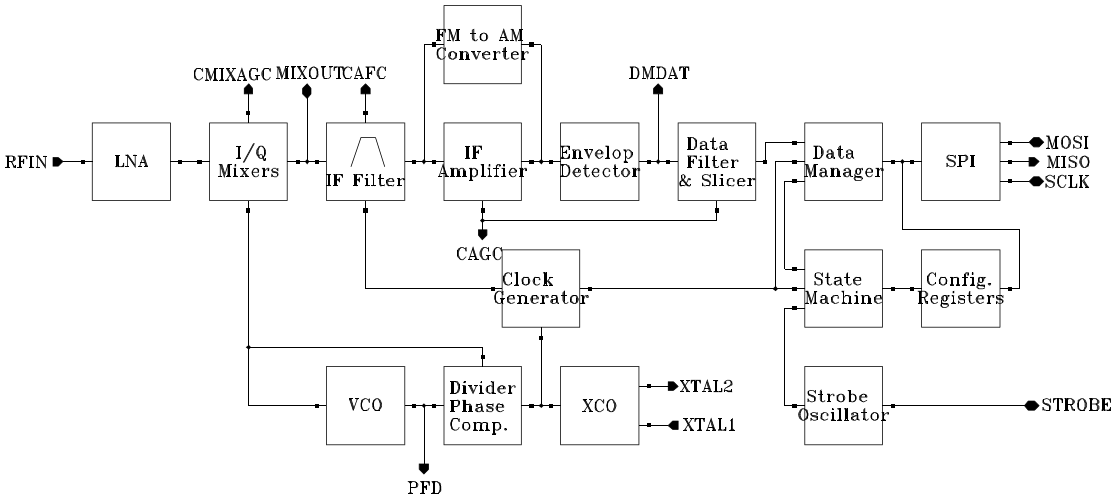

Figure 1. Block diagram

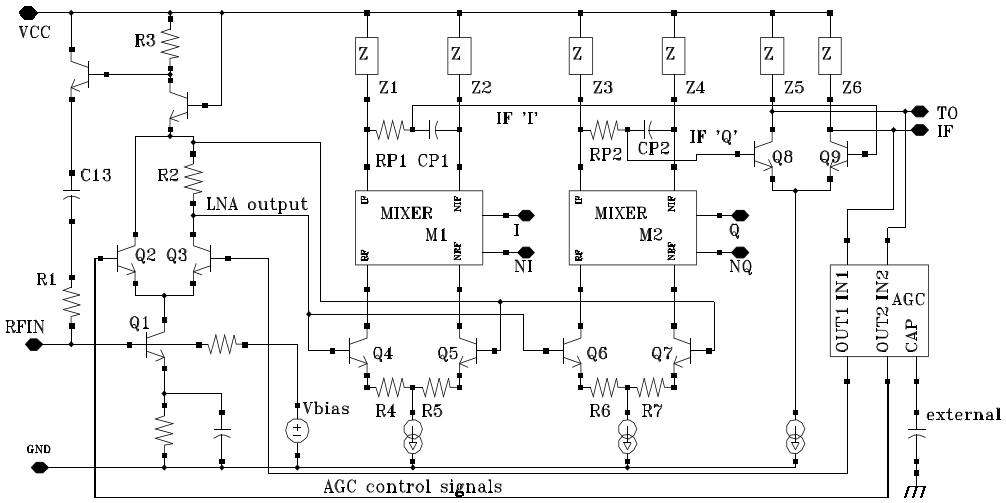

Figure 2. AGC controlled LNA and image cancelling mixer

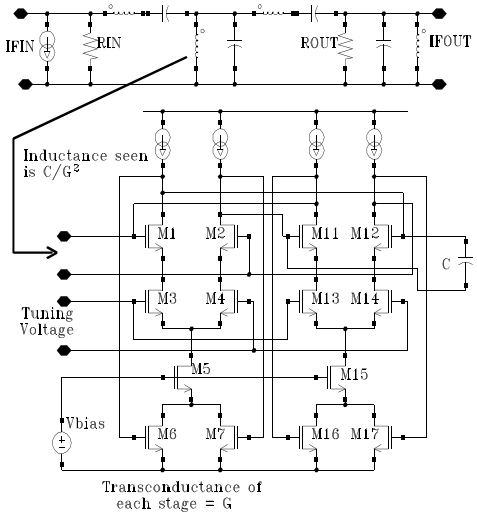

Figure 3. IF filter and gyrator stage

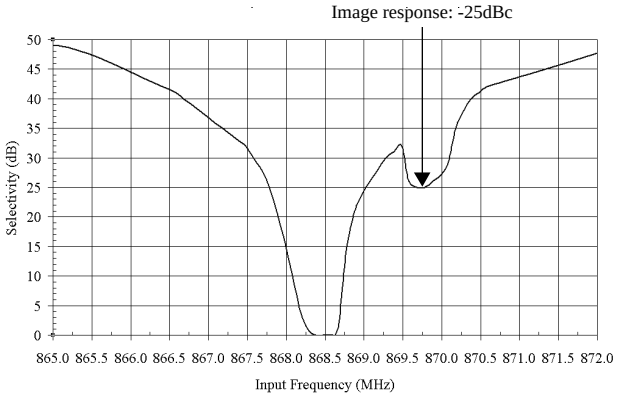

Figure 5. Receiver selectivity versus input frequency

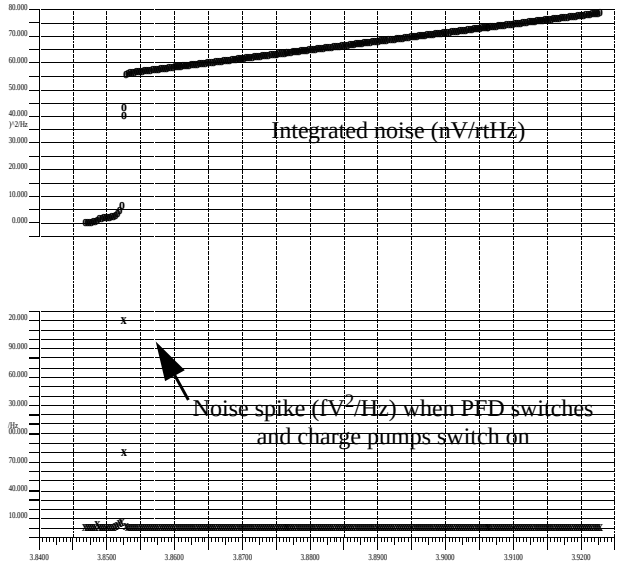

Figure 4. Simulation of PFD noise
in a 74ns period of the crystal oscillator

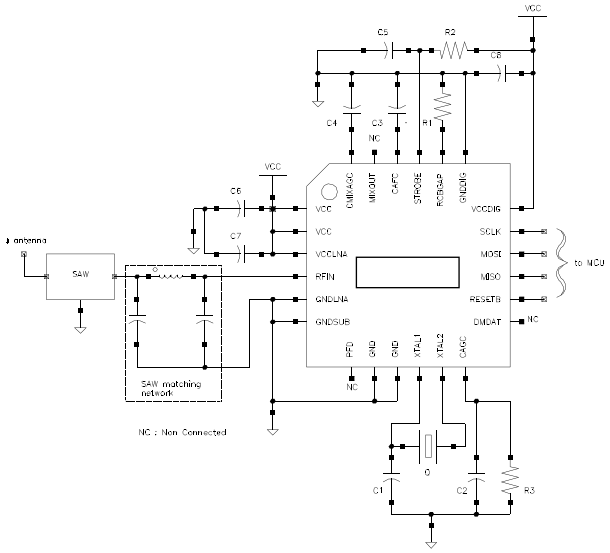

Figure 6. Application schematic